

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 15670-0029US1	Application No. 10/558,842
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)		Applicant Chung-Kuan Cheng, et al.	
		Filing Date January 18, 2007	Group Art Unit
(37 CFR §1.98(b))			

### U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2002/0131135	09/19/2002	Chow et al.			
	AB	2003/0065965	04/03/2003	Korobkov, Alexander			
	AC	2003/0075765	04/24/2003	Ohnakado et al.			
	AD	2003/0200071	10/23/2003	Zhang et al.			
	AE	2003/0204828	10/30/2003	Iwanishi, Nobufusa			
	AF	2004/0008096	01/15/2004	Liu et al.			
	AG	2004/0044510	03/04/2004	Zolotov et al.			
	AH	2005/0076318	04/07/2005	Croix et al.			
	AI	2005/0096888	05/05/2005	Ismail			
	AJ	2005/0102124	05/12/2005	Root et al.			
	AK	5,313,398	05/17/1994	Rohrer et al.			
	AL	5,379,231	01/03/1995	Pillage et al.			
	AM	5,467,291	11/14/1995	Fan et al.			
	AN	5,694,052	12/02/1997	Sawai et al.			
	AO	5,790,415	08/04/1998	Pullela et al.			
	AP	5,888,875	03/30/1999	Lasky			
	AQ	6,141,676	10/31/2000	Ramirez-Angulo et al.			
	AR	6,308,300	10/23/2001	Bushnell et al.			
	AS	6,557,148	04/23/2003	Nishida et al.			
	AT	6,662,149	12/09/2003	Devgan et al.			
	AU	6,665,849	12/16/2003	Meuris et al.			

### Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AV	WO 2007/005005	01/11/2007	WIPO				

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Other Documents (include Author, Title, Date, and Place of Publication)								
Examiner Initial	Desig. ID	Document						
	AW	Acar et al., "TETA: Transistor Level Waveform Evaluation for Timing Analysis," IEEE Trans. On Computer-Aided Design, Volume 21, No. 5, (May 2002)						
	AX	Afshari, E., et al., "Non-Linear Transmission Lines for Pulse Shaping In Silicon," Proc. of IEEE Custom Integrated Circuits Conference, pp. 91-94, Sept. 2003.						
	AY	Backhouse et al., "WSix Thin Film for Resistors," Thin Solid Films, vol. 311, no. 1-2, pp. 299-303 (1997).						
	BA	Beattie, M., et al., "IC Analyses Including Extracted Inductance Models" Proceedings of the 36 <sup>th</sup> ACM/IEEE conference on Design automation. June 21-25, 1999, pp. 915-920 (6 pages). New Orleans, LA, USA.						
	BB	Beckmann, B.M., et al., "TLC: Transmission Line Caches," Proceedings of the 36 <sup>th</sup> IEEE International Symposium on Microarchitecture (MICRO-36'03), 12 pages (2003).						
	BC	Blaauw, D., et al., "Design and Analysis of Power Distribution Networks," Design of high-performance microprocessor circuits, Chapter 24, pp. 499-521, IEEE Press 2001 by the Institute of Electrical and Electronics Engineers, Inc., 3 Park Avenue, 17 <sup>th</sup> Floor, New York, NY, USA.						
	BD	Chang et al., "RF/Wireless Interconnect for Inter- and Intra-Chip Communications," Proceedings of the IEEE, vol. 89, no. 4, pp. 456-466 (2001).						
	BE	Chang et al., "Near Speed-of-Light Signaling Over On-Chip Electrical Interconnects," IEEE Journal of Solid-State Circuits, vol. 38, no. 5, pp. 834-838 (2003).						
	BF	Chen, H., et al., "Surfliner: a distortionless electrical signaling scheme for speed of light on-chip communications," Proceedings of the 2005 International Conference on Computer Design (ICCD '05), 6 pages, (2005).						
	BG	Dally et al., "High-Performance Electrical Signaling," IEEE Integrated Conference on Massively Parallel Processing Using Optical Interconnections, 6 pages, June 1998.						
	BH	Dally, W., "More about Wires Lossy Wires, Multi-Drop Buses, and Balanced Lines," EE273 Lecture 3 (10 pages). September 30, 1998, Computer Systems Laboratory, Stanford University.						
	BI	De Geus, A. J., "SPECS: simulation program for electronic circuits and systems." In Proceedings of the International Symposium on Circuits and Systems, pp. 534-537, May 7-10, 1984. Queen Elizabeth Hotel, Montreal, Canada.						
	BJ	Devgan, A., et al., "Adaptively Controlled Explicit Simulation." IEEE Transactions on Computer-Aided Design of ICs and Systems, vol. CAD-13(6), pp. 746-762, June 1994.						
	BK	Feldman, P., et al., "Reduced-order modeling of large linear subcircuits via a block Lanczos algorithm," Proceedings of 32 <sup>nd</sup> DAC, pp. 474-479, 1995. San Francisco, California. ISBN:0-89791-725-1.						
	BL	Gala, K., et al., "On Chip Inductance Modeling and Analysis," pp. 63-68. Inductance Models, DAC, June 2000. Los Angeles, California						
	BM	He, L., et al., "An Efficient Inductance Modeling for Onchip Interconnects," CICC, May 1999, pp. 457-460. Town and Country Hotel, San Diego, California.						

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**Other Documents (include Author, Title, Date, and Place of Publication)**

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	BN	Ho et al., "The Future of Wires," Proc. of IEEE, vol. 89, no. 4, pp. 490-504 (April 2001).
	BO	Ho, R., et al., "Efficient On-Chip Global Interconnectors," 2003 Symposium on VLSI Circuits Digest of Technical Papers, pp. 271-274, June 2003.
	BP	International Search Report and Written Opinion dated June 2, 2006, for PCT/US05/20369, international filing date June 8, 2005 (9 pages).
	BQ	Jokerst et al., "The Heterogeneous Integration of Optical Interconnections Into Integrated Microsystems," IEEE Journal of Selected Topics in Quantum Electronics, vol. 9, no. 2, pp. 350-360 (March/April 2003)
	BR	Kerns, K.J., et al., "Stable and efficient reduction of substrate model networks using congruence transforms," Proceedings of ICCAD, pp. 207-214, 1995. San Jose, California.
	BS	Krauter, B., et al., "Generating Sparse Partial Inductance Matrices with Guaranteed Stability," Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design. San Jose, California, pp. 45-52 (1995)
	BT	Kuhn et al., "Integration of Mixed-Signal Elements into a High-Performance Digital CMOS Process," Intel Technology Journal, vol. 6, Issue 2, pp. 31-42 (May 16, 2002)
	BU	Lee, Y.M., et al., "The power grid transient simulation in linear time on 3D alternating-direction-implicit method," Proceedings of the Design, Automation and Test in Europe Conference and Exhibition. Pages: 1020 - 1025, (2003).
	BV	Lelarsmee, E., et al., "The Waveform relaxation method for the time-domain analysis of large scale integrated circuits." IEEE Transactions on Computer-Aided Design of ICs and Systems, vol. CAD-1(3), pp. 131-145, July 1982.
	BW	Li, Z., et al., "SILCA: Fast-Yet-Accurate Time-Domain Simulation of VLSI Circuits with Strong Parasitic Coupling Effects," pp. 793-799, ICCAD 2003. San Jose, California.
	BX	Lin, S., "Stepwise equivalent conductance of circuit simulation." IEEE Transactions on Computer-Aided Design of ICs and Systems, vol. CAD-12(5), pp. 672-683, May 1993.
	CA	Lin, S., et al., "Transient simulation of lossy interconnects based on the recursive convolution formulation," IEEE Transactions on CAS I: Fundamental Theory and Applications, vol. 39, pp. 879-892. November 1992.
	CB	Maheshwari, A., et al., "Differential Current-Sensing for On Chip Interconnects," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 12, pp. 1321-1329 (Dec. 2004).
	CC	Namiki, T., et al., "New FDTD algorithm free from the CFL condition restraint for a 2D-TE wave," IEEE Antennas Propagat. Symp. Dig., pp. 192-195, (July 1999).
	CD	Newton, A.R., et al., "Relaxation based electrical simulation." IEEE Transaction on Computer-Aided Designs of ICs and Systems, vol. CAD-3(4), pp. 30-330. October 1984.
	CE	Odabasioglu, A., et al., "PRIMA: Passive Reduced-Order Interconnect Macromodeling Algorithm," Proc. ACM/IEEE ICCAD Nov. 1997, pp. 58-65. San Jose, California.
	CF	Phillips, J.R., et al., "Guaranteed passive balancing transformations for model order reduction," Proceedings of 39 <sup>th</sup> DAC, pp. 52-57, 2002.
	CG	Raghavan, V., et al., "AWESpice: A general tool for the accurate and efficient simulation of interconnect problems," Proceedings of the 29 <sup>th</sup> ACM/IEEE conference on Design Automation, pp. 87-92, June 8-12, 1992. Anaheim, California.

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	CH	Sakallah, K.A., et al., "SAMSON2: an event driven VLSI circuit simulator." IEEE Transactions on Computer-Aided Design of ICs and Systems, vol. 4(4), pp. 668-684. October 1985.
	CI	Stojanovic, V. et al., "Adaptive Equalization and Data Recovery in a Dual Mode (PAM2/4) Serial Link Transceiver," 2004 Symposium on VLSI Circuits Digest of Technical Papers, pp. 348-351 (2004)
	CJ	Visweswariah, C., et al., "Piecewise Approximate Circuit Simulation." IEEE Transactions on Computer-Aided Design of ICs and Systems, vol. CAD-10(7), pp. 861-870, July 1991.
	CK	Wachspress, et al., "An alternating-direction implicit iteration technique," J. Soc. Ind. and Appl. Math 8: 403-424 (1960).
	CL	White, J., et al., "RELAX2: a new waveform relaxation approach for the analysis of LSI MOS circuits." In Proceedings of the International Symposium on Circuits and Systems (ISCAS), pp. 756-759, vol. 2. May 1983. Newport Beach, California.
	CM	Zheng et al., "Toward the development of a three-dimensional unconditionally stable finite-difference time domain method," IEEE Tran. Microwave Theory and Techniques, vol. 48, no. 9, (9 pages). Sept. 2000.
	CN	Zhu, et al., "Efficient Transient Simulation for Transistor-Level Analysis." EDA Technofair Design Automation Conference Asia and South Pacific Proceedings of the 2005 Conference on Asia South Pacific Design Automation, Shanghai, China (2005) pp. 240-243, published by the ACM, New York, NY, USA.

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